

# **METHOD OF MANUFACTURING A FLIP-CHIP TYPE SEMICONDUCTOR DEVICE WITH A STRESS-ABSORBING LAYER MADE OF THERMOSETTING RESIN**

## **CROSS-REFERENCE TO RELATED PATENT APPLICATIONS**

**[0001]** This application is a division of Application No. 09/704,521, filed November 3, 2000, now pending, and based on Japanese Patent Application No. 11-313684, filed November 4, 1999, by Hirokazu HONDA. This application claims only subject matter disclosed in the parent application and therefore presents no new matter.

## **BACKGROUND OF THE INVENTION**

### **Field of the Invention**

**[0002]** The present invention relates to a flip-chip type semiconductor device and its manufacturing method, and more particularly, to the improvement of reducing stress strain within the flip-chip type semiconductor device.

### **Description of the Related Art**

**[0003]** Recently, flip-chip type semiconductor devices have been developed to meet the requirements of higher performance, smaller and lighter size and higher speed for electronic equipment.

**[0004]** Generally, a flip-chip type semiconductor device having metal bumps is directly mounted on a motherboard having electrodes corresponding to the metal bumps. That is, if the metal bumps are solder balls, the solder balls are reflowed and soldered on the motherboard. In this case, a stress strain occurs due to the discrepancy in thermal expansion coefficient between the semiconductor device and the motherboard, which would deteriorate the reliability characteristics of the semiconductor device. This will be explained later in detail.

**[0005]** In order to minimize the above-mentioned discrepancy in thermal expansion coefficient, the motherboard is made of ceramic material such as aluminum nitride (AlN), mullite or glass ceramics, which have a thermal expansion coefficient close to

that of silicon. In this case, however, the motherboard becomes more expensive, and therefore, its application is limited to high-priced equipment such as a super computer and a large scale computer.

**[0006]** On the other hand, in order to disperse shearing stress occurring at the metal bumps to substantially reduce the above-mentioned stress strain, under-fill resin is inserted between the semiconductor device and the motherboard (see JP-A-9-92685). In this case, however, if voids may be generated within the under-fill resin or if the adhesive characteristics between the under-fill resin and the semiconductor device (or the motherboard) deteriorate, the semiconductor device would be separated from the motherboard.

**[0007]** In other approaches to disperse shearing stress occurring at the metal bumps to substantially reduce the above-mentioned stress strain, an elastic layer made of rubber or expandable styrene is provided on the semiconductor device (see JP-A-11-40613, JP-A-11-74309). This also will be explained later in detail.

**[0008]** In the above-mentioned approaches, however, since the elastic layer includes much contamination, the reliability of the semiconductor device would deteriorate.

### **SUMMARY OF THE INVENTION**

**[0009]** It is an object of the present invention to provide a reliable flip-chip type semiconductor device and its manufacturing method.

**[0010]** According to the present invention, in a flip-chip type semiconductor device, a plurality of pad electrodes are formed on a semiconductor substrate. An insulating stress-absorbing resin layer made of thermosetting resin is formed on the semiconductor substrate and has openings corresponding to the pad electrodes. A plurality of flexible conductive members are filled in the openings. A plurality of metal bumps are formed on the flexible conductive layers.

**[0011]** Since the thermosetting resin has little contamination, the reliability of the flip-chip type semiconductor device would be improved.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0012]** The present invention will be more clearly understood from the description set forth below, as compared with the prior art, with reference to the accompanying drawings, wherein:

**[0013]** Figs. 1A, 1B and 1C are views for explaining a prior art method for mounting a flip-chip type semiconductor device on a motherboard;

**[0014]** Figs. 2A through 2J are cross-sectional views for explaining a first embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention;

**[0015]** Fig. 3 is a plan view of one flip-chip type semiconductor device obtained by the method as illustrated in Figs. 2A through 2J;

**[0016]** Fig. 4 is a detailed plan view of the flip-chip type semiconductor device of Fig. 3;

**[0017]** Figs. 5A through 5F are cross-sectional views for explaining a second embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention;

**[0018]** Figs. 6A through 6N are cross-sectional views for explaining a third embodiment of the method for manufacturing a flip-chip type semiconductor device;

**[0019]** Fig. 7 is a plan view of one flip-chip type semiconductor device obtained by the method as illustrated in Figs. 6A through 6N;

**[0020]** Figs. 8A through 8N are cross-sectional views for explaining a fourth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention;

**[0021]** Figs. 9A, 9B and 9C are cross-sectional views illustrating a modification of the third embodiment as illustrated in Figs. 6A through 6N;

**[0022]** Figs. 10A, 10B and 10C are cross-sectional views illustrating a modification of the fourth embodiment as illustrated in Figs. 8A through 8N;

**[0023]** Figs. 11A through 11E are cross-sectional views illustrating another modification of the third and fourth embodiments as illustrated in Figs. 6A through 6N and Figs. 8A through 8N;

**[0024]** Figs. 12A through 12E are cross-sectional views illustrating another modification of the third and fourth embodiments as illustrated in Figs. 6A through 6N and Figs. 8A through 8N;

**[0025]** Figs. 13A through 13M are cross-sectional views for explaining a fifth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention; and

**[0026]** Figs. 14A through 14Q are cross-sectional views for explaining a sixth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention.

### **DESCRIPTION OF THE PREFERRED EMBODIMENTS**

**[0027]** Before the description of the preferred embodiments, prior art flip-chip type semiconductor devices will be explained with reference to Figs. 1A, 1B and 1C.

**[0028]** Figs. 1A, 1B and 1C are views for explaining a prior art method for mounting a flip-chip type semiconductor device on a motherboard.

**[0029]** First referring to Fig. 1A, a flip-chip type semiconductor device 101 having metal bumps 102 and a motherboard 103 having electrodes (not shown) corresponding to the metal bumps 102 are prepared. Note that the motherboard 103 is prepared by a user.

**[0030]** Next, referring to Fig. 1B, the flip-chip type semiconductor device 101 is mounted on the motherboard 103. Note that, if the metal bumps 102 are solder balls, the solder balls are reflowed at a temperature below a predetermined temperature and soldered on the motherboard 103. In this case, a stress strain occurs due to the

discrepancy in thermal expansion coefficient between the semiconductor device 101 and the motherboard 103, which would deteriorate the reliability characteristics of the semiconductor device 101.

**[0031]** In order to minimize the discrepancy in thermal expansion coefficient between the semiconductor device 101 and the motherboard 103, the motherboard 103 may be made of ceramic material such as aluminum nitride (AlN), mullite or glass ceramics, which have a thermal expansion coefficient close to that of silicon. In this case, however, the motherboard 103 becomes more expensive, and therefore, its application is limited to high-priced equipment such as a super computer and a large scale computer.

**[0032]** On the other hand, in order to disperse shearing stress occurring at the metal bumps 102 to substantially reduce the above-mentioned stress strain, under-fill resin is inserted between the semiconductor device 101 and the motherboard 103 (see JP-A-9-92685). In JP-A-9-92685, note that under-fill is inserted between a flip-chip type semiconductor device and an interposer substrate. In this case, however, if voids may be generated within the under-fill resin or if the adhesive characteristics between the under-fill resin and the semiconductor device 101 (or the motherboard 103) deteriorate, the semiconductor device 101 would be separated from the motherboard 103.

**[0033]** In other approaches to disperse shearing stress occurring at the metal bumps 102 to substantially reduce the above-mentioned stress strain, an elastic layer made of rubber or expandable styrene is provided on the semiconductor device (see JP-A-11-40613, JP-A-11-74309).

**[0034]** In the state as illustrated in Fig. 1B, if an open state or a short-circuit state is generated by a defective soldering process, the semiconductor device 101 is separated and detached by a special heating tool 104 as illustrated in Fig. 1C. In this case, the metal bumps 102 are damaged. Therefore, the metal bumps 102 are repaired, and the semiconductor device 101 can be reused.

[0035] However, in a case where under-fill resin is used, the semiconductor device 101 per se may be damaged, so that it is impossible to reuse the semiconductor device 101. Additionally, the motherboard 103 may also be damaged.

[0036] Further, in a case where an elastic layer is made of rubber or expansible styrene, since the elastic layer includes much contamination, the reliability of the semiconductor device 101 would deteriorate.

[0037] A first embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 2A through 2J.

[0038] First, referring to Fig. 2A, pad electrodes 12 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 11. Then, a passivation layer 13 made of non-organic material such as silicon oxide ( $\text{SiO}_2$ ) or organic material such as polyimide is deposited on the silicon substrate 11 to protect active areas thereof.

[0039] Next, referring to Fig. 2B, an insulating stress-absorbing resin layer 14 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 14 is approximately from 0.01 to 8 GPa.

[0040] Next, referring to Fig. 2C, a photoresist layer is coated on the insulating stress-absorbing resin layer 14 and is patterned by a photolithography process to form a photoresist pattern layer 15 which has openings corresponding to the pad electrodes 12.

[0041] Next, referring to Fig. 2D, the insulating stress-absorbing resin layer 14 is perforated by a wet etching process, a plasma etching process or a laser process using the photoresist pattern layer 15 as a mask, to form openings 14a, thus exposing the pad electrodes 12. Note that, if the insulating stress-absorbing resin layer 14 is made of material which can be subjected to a chemical etching process, the wet etching process can be used. On the other hand, if the insulating stress-absorbing resin layer

14 is made of material which cannot be subjected to a chemical etching process, the plasma etching process or the laser process can be used.

**[0042]** Next, referring to Fig. 2E, the photoresist pattern layer 15 is removed to expose the insulating stress-absorbing resin layer 14. Then, the device is subjected to a plasma surface treatment using inert gas such as Ar gas under a low pressure atmosphere. As a result, the remainder of the insulating stress-absorbing resin layer 14 on the pad electrodes 12 is completely removed, and also metal oxide on the surface of the pad electrodes is removed.

**[0043]** Next, referring to Fig. 2F, a flexible conductive layer 16 is coated on the insulating stress-absorbing resin layer 14 by a screen printing method or the like, so that the flexible conductive layer 16 is filled in the openings 14a, thus preventing the pad electrodes 12 from being oxidized. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

**[0044]** Next, referring to Fig. 2G, the flexible conductive layer 16 is flattened by a chemical mechanical polishing (CMP) process, so that the flexible conductive layer 16 is filled only in the openings 14a. In this case, a plasma surface treatment may be carried out to remove polishing waste caused by the CMP process.

**[0045]** Next, referring to Fig. 2H, an electroless Cu plating process or an electroless Ni plating process is carried out to form land portions (not shown) on the pad electrodes 12. The land portions can be formed by carrying out an electroless Au plating process after an electrolytic Cu plating process. Then, metal bumps (solder balls) 17 made of Sn and Pb are soldered to the pad electrodes 12 via the land portions. Thus, since the land portions improves the wettability of the metal bumps 17, the metal bumps 17 can be securely adhered to the pad electrodes 12.

**[0046]** In to Fig. 2H, flux (not shown) instead of the land portions can be coated on the pad electrodes 12, and then, metal bumps 17 are soldered to the pad electrodes 12

and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 17 can be securely adhered to the pad electrodes 12.

[0047] Note that the metal bumps 17 can be made of Au or Sn-Ag alloy.

[0048] Next, referring to Fig. 2I, the device is cut by a dicing blade 18 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 2J.

[0049] One of the flip-chip type semiconductor chips obtained by the manufacturing method as illustrated in Figs. 2A through 2J is illustrated in Fig. 3. In Fig. 3, the pad electrodes 12 are arranged at the periphery of the flip-chip type semiconductor chip and are surrounded by the insulating stress-absorbing resin layer 14, and the metal bumps 17 are arranged on the pad electrodes 12. Actually, the number of the pad electrodes 12 is very large as illustrated in Fig. 4.

[0050] According to the above-described first embodiment, since the insulating stress-absorbing resin layer 14 and the flexible conductive layer 16 disperse shearing stress occurring at the metal bumps 17, the reliability of the flip-chip type semiconductor device would be improved. Additionally, since the insulating stress-absorbing resin layer 14 is made of thermosetting resin which includes little contamination, the flip-chip type semiconductor device would be further improved.

[0051] A second embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 5A through 5F.

[0052] After the steps as illustrated in Figs. 2A through 2D of the first embodiment are carried out, referring to Fig. 5A, conductive wire 21 made of Au or Cu is connected to the pad electrodes 12 via conductive adhesives (not shown) by a wire bonding process.

[0053] Next, referring to Fig. 5B, in a similar way to those of Fig. 2F, a flexible conductive layer 16 is coated on the insulating stress-absorbing resin layer 14 by a screen printing method or the like, so that the flexible conductive layer 16 is filled in



the openings 14a, to completely cover the conductive wire 21. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

**[0054]** Next, referring to Fig. 5C, in the same way in Fig. 2G, the flexible conductive layer 16 is flattened by a CMP process, so that the flexible conductive layer 16 is filled only in the openings 14a. In this case, a plasma surface treatment may be carried out to remove polishing waste caused by the CMP process.

**[0055]** Next, referring to Fig. 5D, in the same way as in Fig. 2H, an electroless Cu plating process or an electroless Ni plating process is carried out to form land portions (not shown) on the pad electrodes 12. The land portions can be formed by carrying out an electroless Au plating process after an electrolytic Cu plating process. Then, metal bumps (solder balls) 17 made of Sn and Pb are soldered to the pad electrodes 12 via the land portions. Thus, since the land portions improves the wettability of the metal bumps 17, the metal bumps 17 can be securely adhered to the pad electrodes 12.

**[0056]** Even in Fig. 5D, in the same way as in Fig. 2H, flux (not shown) instead of the land portions can be coated on the pad electrodes 12, and then, metal bumps 17 are soldered to the pad electrodes 12 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 17 can be securely adhered to the pad electrodes 12.

**[0057]** Note that the metal bumps 17 can be made of Au or Sn-Ag alloy.

**[0058]** Next, referring to Fig. 5E, in the same way as in Fig. 2I, the device is cut by a dicing blade 18 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 5F.

**[0059]** Thus, in the second embodiment, the metal bumps 17 can be more surely electrically-connected to the pad electrodes 12 due to the presence of the conductive wire 21 as compared with the first embodiment.

[0060] A third embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 6A through 6N.

[0061] First, referring to Fig. 6A, in the same way as in Fig. 2A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 33 made of non-organic material such as silicon oxide ( $\text{SiO}_2$ ) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

[0062] Next, referring to Fig. 6B, in the same way as in Fig. 2B, an insulating stress-absorbing resin layer 34 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 34 is approximately from 0.01 to 8 GPa.

[0063] Next, referring to Fig. 6C, a Cu layer 35 is deposited on the insulating stress-absorbing resin layer 34.

[0064] Note that other metal such as nickel can be used for the layer 35.

[0065] Next, referring to Fig. 6D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 36.

[0066] Next, referring to Fig. 6E, an Au plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

[0067] Note that other metal such as nickel can be used for the layer 37.

[0068] Next, referring to Fig. 6F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

**[0069]** Next, referring to Fig. 6G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

**[0070]** Next, referring to Fig. 6H, a photoresist pattern layer 37', which has openings corresponding to the pad electrodes 32, is formed by a photolithography process.

**[0071]** Next, referring to Fig. 6I, the insulating stress-absorbing resin layer 34 is etched by using the photoresist pattern layer 38 as a mask, to form openings 34a in the insulating stress-absorbing resin layer 34.

**[0072]** Next, referring to Fig. 6J, the photoresist pattern layer 38 is removed.

**[0073]** Next, referring to Fig. 6K, a flexible conductive layer 38 is coated by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the openings 34a, thus preventing the pad electrodes 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 37 are electrically connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 38 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

**[0074]** Note that a solder-resist layer or a resin layer can be coated on the portions of the Au layer 37 where metal bumps will be formed. Thus, the Au layer 37 can be protected by the solder-resist layer or the resin layer to improve the waterproof characteristics thereof.

**[0075]** Referring to Fig. 6L, metal bumps 39 are soldered to the Au layer 37 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the Au layer 37.

**[0076]** Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

**[0077]** Next, referring to Fig. 6M, the device is cut by a dicing blade 40 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 6N.

**[0078]** One of the flip-chip type semiconductor chips obtained by the manufacturing method as illustrated in Figs. 6A through 6N is illustrated in Fig. 7. In Fig. 7, although the pad electrodes 32 are arranged at the periphery of the flip-chip type semiconductor chip and then surrounded by the insulating stress-absorbing resin layer 34 in the same way as in the first embodiment, the metal bumps 39 are arranged in an inner area of the flip-chip type semiconductor chip as compared with the metal bumps 25 of Fig. 3, which would prevent the metal bumps 39 from being short-circuited.

**[0079]** A fourth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 8A through 8N.

**[0080]** First, referring to Fig. 8A, in the same way as in Fig. 6A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 32 made of non-organic material such as silicon oxide ( $\text{SiO}_2$ ) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

**[0081]** Next, referring to Fig. 8B, in the same way as in Fig. 6B, an insulating stress-absorbing resin layer 34 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 34 is approximately from 0.01 to 8 GPa.

**[0082]** Next, referring to Fig. 8C, a photoresist pattern layer 41, which has openings corresponding to the pad electrodes 32, is formed by a photolithography process.

**[0083]** Next, referring to Fig. 8D, the insulating stress-absorbing resin layer 34 is etched by using the photoresist pattern layer 41 as a mask. As a result, openings 34a

corresponding to the pad electrodes 32 are perforated in the insulating stress-absorbing resin layer 34.

**[0084]** Next, referring to Fig. 8E, the photoresist pattern layer 41 is removed.

**[0085]** Next, referring to Fig. 8F, in a similar way to that of Fig. 6C, a Cu layer 35 is formed on the insulating stress-absorbing resin layer 34 by using a film laminating method or a pressing method.

**[0086]** Note that other metal such as nickel can be used for the layer 35.

**[0087]** Next, referring to Fig. 8G, in the same way as in Fig. 6D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 36.

**[0088]** Next, referring to Fig. 8H, in the same way as in Fig. 6E, an Au plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

**[0089]** Note that other metal such as nickel can be used for the layer 37.

**[0090]** Next, referring to Fig. 8I, in the same way as in Fig. 6F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

**[0091]** Next, referring to Fig. 8J, in the same way as in Fig. 6G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

**[0092]** Next, referring to Fig. 8K, in the same way as in Fig. 6K, a flexible conductive layer 38 is coated on the insulating stress-absorbing resin layer 34 by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the openings 34a, thus preventing the pad electrodes 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 37 are electrically connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that

shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

**[0093]** Note that a solder-resist layer or a resin layer can be coated on the portions of the Au layer 37 where metal bumps will be formed. Thus, the Au layer 37 can be protected by the solder-resist layer or the resin layer to improve the waterproof characteristics.

**[0094]** Referring to Fig. 8L, in the same way as in Fig. 6L, metal bumps 39 are soldered to the pad electrodes 32 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the pad electrodes 32.

**[0095]** Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

**[0096]** Next, referring to Fig. 8M, in the same way as in Fig. 6M, the device is cut by a dicing blade 40 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 8N.

**[0097]** In the fourth embodiment, although the steps as illustrated in Figs. 8C and 8D are added to the third embodiment, the steps as illustrated in Figs. 6H, 6I and 6J of the third embodiment are omitted, which would decrease the manufacturing cost.

**[0098]** A modification of the third embodiment of the present invention will be explained next with reference to Figs. 9A through 9C.

**[0099]** First, referring to Fig. 9A, in the same way as in Fig. 6A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 32 made of non-organic material such as silicon oxide (SiO<sub>2</sub>) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

**[0100]** Next, referring to Fig. 9B, a resin coated copper (RCC) layer consisting of an insulating stress-absorbing resin layer 34 laminated by a Cu layer 35 is prepared.

**[0101]** Next, referring to Fig. 9C, the RCC layer (34, 35) is adhered to the pad electrodes 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34, 35) has good adhesive characteristics, the RCC layer (34, 35) per se can be easily adhered to the pad electrodes 32 and the passivation layer 33.

**[0102]** After that, the steps as illustrated in Figs. 6D through 6N are carried out to complete a flip-chip type semiconductor chip.

**[0103]** A modification of the fourth embodiment of the present invention will be explained next with reference to Figs. 9A through 9C.

**[0104]** First, referring to Fig. 10A, in the same way as in Fig. 8A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 32 made of non-organic material such as silicon oxide ( $\text{SiO}_2$ ) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

**[0105]** Next, referring to Fig. 10B, an RCC layer consisting of an insulating stress-absorbing resin layer 34 laminated by a Cu layer 35 is prepared. In this case, openings 34a are perforated in the insulating stress-absorbing resin layer 34 in advance by an etching process or the like.

**[0106]** Next, referring to Fig. 10C, the RCC layer (34, 35) is adhered to the pad electrodes 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34, 35) has good adhesive characteristics, the RCC layer (34, 35) per se can be easily adhered to the pad electrodes 32 and the passivation layer 33.

**[0107]** After that, the steps as illustrated in Figs. 8G through 8N are carried out to complete a flip-chip type semiconductor chip.

**[0108]** Another modification of the third and fourth embodiments of the present invention will be explained next with reference to Figs. 11A through 11E. After the

steps of Figs. 6A through 6J or the steps of Figs. 8A through 8J are carried out, the steps of Figs. 11A through 11E are carried out.

**[0109]** First, referring to Fig. 11A, conductive wiring 51 made of Au or Cu is formed by using a wire bonding process, to electrically connect the pad electrodes 32 to the Cu layer 35 and the Au layer 37. Note that, the pad electrodes 32 are subjected to a plasma surface treatment before the wire bonding process, to remove etching remainder of the insulating stress-absorbing resin layer 34 on the pad electrodes 32 and oxide thereon, which would improve the wire bonding characteristics.

**[0110]** Next, referring to Fig. 11B, metal bumps 39 are soldered to the pad electrodes 32 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the pad electrodes 32.

**[0111]** Next, referring to Fig. 11C, an insulating resin layer 52 is filled in the openings 34a, to mechanically and chemically protect the conductive wiring 51 as well as to enhance the water-vapor proof characteristics.

**[0112]** The insulating resin layer 52 can be made of the same or similar material as that of the insulating stress-absorbing resin layer 34. If the insulating resin layer 52 is liquid, a partial coating process is performed upon the conductive wiring 51 by a potting method. On the other hand, if the insulating resin layer 52 is solid, the conductive wiring 51 can be partially sealed by a transfer sealing method using metal molds.

**[0113]** Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

**[0114]** Next, referring to Fig. 11D, the device is cut by a dicing blade 40 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 11E.

**[0115]** A further modification of the third and fourth embodiments of the present invention will be explained next with reference to Figs. 12A through 12E. After the steps of Figs. 6A through 6J or the steps of Figs. 8A through 8J are carried out, the steps of Figs. 12A through 12E are carried out.



[0116] First, referring to Fig. 12A, a conductive layer 61 made of Zn or NiSn is formed by using an electroless plating and etching process, to electrically connect the pad electrodes 32 to the Cu layer 35 and the Au layer 37. Note that the conductive layer 61 can be formed by adhering L-shaped conductive members made of Cu, Ni or their alloy by conductive adhesives.

[0117] Next, referring to Fig. 12B, in the same way as in Fig. 11B metal bumps 39 are soldered to the pad electrodes 32 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the pad electrodes 32.

[0118] Next, referring to Fig. 12C, in the same way as in Fig. 11C, an insulating resin layer 52 is filled in the openings 34a, to mechanically and chemically protect the conductive wiring 51 as well as to enhance the water-vapor proof characteristics.

[0119] The insulating resin layer 52 can be made of the same or similar material as that of the insulating stress-absorbing resin layer 34. If the insulating resin layer 52 is liquid, a partial coating process is performed upon the conductive wiring 51 by a potting method. On the other hand, if the insulating resin layer 52 is solid, the conductive wiring 51 can be partially sealed by a transfer sealing method using metal molds.

[0120] Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

[0121] Next, referring to Fig. 12D, in the same way as in Fig. 11D, the device is cut by a dicing blade 40 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 12E.

[0122] A fifth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 13A through 13N.

[0123] First, referring to Fig. 13A, in the same way as in Fig. 9A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a

passivation layer 33 made of non-organic material such as silicon oxide ( $\text{SiO}_2$ ) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

[0124] Next, referring to Fig. 13B, an RCC layer consisting of a photosensitive insulating stress-absorbing resin layer 34' laminated by a Cu layer 35 is prepared. The photosensitive insulating stress-absorbing layer 34' is made of the above-mentioned thermosetting resin combined with a photosensitive material such as bis(azide) compound or thiodiazo-naphthoquinone compound.

[0125] Next, referring to Fig. 13C, in the same way as in Fig. 9C, the RCC layer (34', 35) is adhered to the pad electrodes 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34', 35) has good adhesive characteristics the RCC layer (34', 35) per se can be easily adhered to the pad electrodes 32 and the passivation layer 33.

[0126] Next, referring to Fig. 13D, in the same way as in Fig. 6D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 36.

[0127] Next, referring to Fig. 13E, in the same way as in Fig. 6E, an Au plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

[0128] Note that other metal such as nickel can be used for the layer 37.

[0129] Next, referring to Fig. 13F, in the same way as in Fig. 6F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

[0130] Next, referring to Fig. 13G, in the same way as in Fig. 6G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

[0131] Next, referring to Fig. 13H, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 71 corresponding to the pad electrode 32. As a

result, if the photosensitive insulating stress-absorbing resin layer 34' is negative, the exposed portions 34'a thereof are hardened.

[0132] Next, referring to Fig. 13I, a solder resist layer 72 is coated on the entire surface.

[0133] Next, referring to Fig. 13J, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 73 corresponding to the pad electrode 32 and a metal bump which will be formed later. As a result, if the solder resist layer 72 is negative, the exposed portions 72a thereof are hardened.

[0134] Next, referring to Fig. 13K, the device is subjected to a developing process, i.e., a chemical etching process using tetraethyl ammonium hydroxide (TMAH) solution. As a result, the unexposed portion of the photosensitive insulating stress-absorbing resin layer 34' and the unexposed portion of the solder resist layer 72 are simultaneously removed. Thus, an opening 34'b is perforated in the photosensitive insulating stress-absorbing resin layer 34', and an opening 72b is perforated in the solder resist layer 72. Then, a high-temperature curing operation is performed upon the device to react the thermosetting components of the photosensitive insulating stress-absorbing resin layer 34' and the solder resist layer 72.

[0135] Next, referring to Fig. 13L, in the same way as in Fig. 6K, a flexible conductive layer 38 is coated by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the openings 34'a, thus preventing the pad electrode 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 37 are electrically connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

[0136] Referring to Fig. 13M, in the same way as in Fig. 6L, metal bumps 39 are soldered to the Au layer 37 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the Au layer 37.

**[0137]** Note that the metal bump 39 can be made of Au or Sn-Ag alloy.

**[0138]** Finally, the device is cut by a dicing blade (not shown) to separate flip-chip type semiconductor chips (pellets) from each other.

**[0139]** In the fifth embodiments as illustrated in Figs. 13A through 13M, since the steps as illustrated in Figs. 6H and 6I are unnecessary, the manufacturing steps can be simplified.

**[0140]** In the fifth embodiment, the steps of Figs. 6B and 6C can be used instead of the steps of Figs. 13B and 13C. Also, the conductive wiring 51 of Figs. 11A through 11E or the conductive layer 61 of Figs. 12A through 12E can be used instead of the conductive layer 38.

**[0141]** A sixth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 14A through 14N.

**[0142]** First, referring to Fig. 14A, in the same way as in Fig. 8A, a pad electrode 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 33 made of non-organic material such as silicon oxide ( $\text{SiO}_2$ ) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

**[0143]** Next, referring to Fig. 14B, in the same way as in Fig. 8B, an insulating stress-absorbing resin layer 34 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 34 is approximately from 0.01 to 8 GPa.

**[0144]** Next, referring to Fig. 14C, in the same way as in Fig. 8C, a photoresist pattern layer 41, which has an opening corresponding to the pad electrode 32, is formed by a photolithography process.

**[0145]** Next, referring to Fig. 14D, in the same way as in Fig. 8D, the insulating stress-absorbing resin layer 34 is etched by using the photoresist pattern layer 41 as a mask. As a result, an opening 34a corresponding to the pad electrode 32 is perforated in the insulating stress-absorbing resin layer 34.

**[0146]** Next, referring to Fig. 14E, in the same way as in Fig. 8E, the photoresist pattern layer 41 is removed.

**[0147]** Note that, if the insulating stress-absorbing resin layer 34 is photosensitive, the steps of Figs. 14C, 14D and 14E are replaced by an ultraviolet exposing and developing process.

**[0148]** Next, referring to Fig. 14F, in the same way as in Fig. 13B, an (RCC) layer consisting of a photosensitive insulating stress-absorbing resin layer 34' laminated by a Cu layer 35 is prepared.

**[0149]** Next, referring to Fig. 14G, in the same way as in Fig. 13C, the RCC layer (34', 35) is adhered to the pad electrode 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34', 35) has good adhesive characteristics the RCC layer (34', 35) per se can be easily adhered to the pad electrode 32 and the passivation layer 33.

**[0150]** Next, referring to Fig. 14H, in the same way as in Fig. 13D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 36.

**[0151]** Next, referring to Fig. 14I, in the same way as in Fig. 13E, an Au plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

**[0152]** Note that other metal such as nickel can be used for the layer 37.

**[0153]** Next, referring to Fig. 14J, in the same way as in Fig. 13F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

**[0154]** Next, referring to Fig. 14K, in the same way as in Fig. 13G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

**[0155]** Next, referring to Fig. 14L, in the same way as in Fig. 13H, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 71 corresponding to the pad electrode 32. As a result, if the photosensitive insulating stress-absorbing resin layer 34' is negative, the exposed portions 34'a thereof are hardened.

**[0156]** Next, referring to Fig. 14M, in the same way as in Fig. 13I, a solder resist layer 72 is coated on the entire surface.

**[0157]** Next, referring to Fig. 14N, in the same way as in Fig. 13I, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 73 corresponding to the pad electrode 32 and a metal bump which will be formed later. As a result, if the solder resist layer 72 is negative, the exposed portions 72a thereof are hardened.

**[0158]** Next, referring to Fig. 14O, in the same way as in Fig. 13J, the device is subjected to a developing process, i.e., a chemical etching process using TMAH solution. As a result, the unexposed portion of the photosensitive insulating stress-absorbing resin layer 34' and the unexposed portion of the solder resist layer 72 are simultaneously removed. Thus, an opening 34'b leading to the opening 34a is perforated in the photosensitive insulating stress-absorbing resin layer 34', and an opening 72b is perforated in the solder resist layer 72. Then, a high-temperature curing operation is performed upon the device to react the thermosetting components of the photosensitive insulating stress-absorbing resin layer 34' and the solder resist layer 72.

**[0159]** Next, referring to Fig. 14P, in the same way as in Fig. 13K, a flexible conductive layer 38 is coated by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the opening 34'b as well as in the opening 34a, thus preventing the pad electrode 32 from being oxidized. As a result,

the Cu layer 35 and the Au layer 37 are electrically connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

**[0160]** Referring to Fig. 14Q, in the same way as in Fig. 13L, metal bumps 39 are soldered to the Au layer 37 and a heating reflowing process is performed thereupon. Even in this case, the metal bump 39 can be securely adhered to the Au layer 37.

**[0161]** Note that the metal bump 39 can be made of Au or Sn-Ag alloy.

**[0162]** Finally, the device is cut by a dicing blade (not shown) to separate flip-chip type semiconductor chips (pellets) from each other.

**[0163]** In the sixth embodiments as illustrated in Figs. 14A through 14L, since the insulating stress-absorbing resin layer (34, 34') is much thicker than the insulating stress-absorbing resin layer 34' in the fifth embodiment, the stress strain due to the discrepancy in thermal expansion coefficient between the device and a motherboard or the like can be remarkably reduced.

**[0164]** As explained hereinabove, according to the present invention, since an elastic layer for reducing the stress strain due to the discrepancy in thermal expansion coefficient is made of thermosetting resin with little contamination, the reliability of flip-chip type semiconductor devices can be improved.